AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-36 (cancelled)

37. (Currently amended) An integrated semiconductor structure comprising:

a multijunction solar cell structure having at least first and second subcells; and

a bypass device integral to a subcell for passing current when the solar cell is shadowed and having p-type, i-type, and n-type layers; wherein

the bypass device and the subcell have an identical ~~sequences~~ sequence of semiconductor layers where each layer in the bypass device has substantially the same composition and thickness as the corresponding layer in the subcell ~~with substantially the same thickness~~ and form an integral semiconductor body.

38. (Previously submitted) The structure as defined in claim 37, wherein said structure includes a substrate, wherein the subcells are formed on a first portion of the substrate and said bypass device includes a bypass diode formed on a second portion of the substrate.

39. (Previously submitted) The structure as defined in claim 38, wherein layers of the subcells are epitaxially grown in a first process and active layers of said bypass diode are epitaxially grown over the layers of the subcells in a subsequent second process.

40. (Previously submitted) The structure as defined in claim 39, wherein said epitaxially grown diode is electrically connected across at least said first and second subcells to protect such first and second subcells against reverse biasing.

41. (Previously submitted) The structure as defined in claim 39, wherein the bypass diode includes a metal/semiconductor contact.

42. (Previously submitted) The structure as defined in claim 41, wherein the metal/semiconductor contact is TiAu with InGaP.

43. (Previously submitted) The structure as defined in claim 41, wherein the metal/semiconductor contact forms a Schottky junction.

44. (Previously submitted) The structure as defined in claim 38, wherein the substrate is Ge.

45. (Currently amended) The structure as defined in claim 37, wherein the second solar subcell is fabricated at ~~as~~ least in part with InGaP.

46. (Previously submitted) The structure as defined in claim 37, wherein the first solar subcell is fabricated at least in part with GaAs.

47. (Previously submitted) A solar cell semiconductor device comprising:

a semiconductor body having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiconductor material forms a sequence of cells of a multijunction solar cell with the top layer of the top cell having a first polarity; and

a second region laterally spaced apart from said first region and in which the sequence of layers forms a support for an integral bypass diode to protect said sequence of cells against reverse biasing at less than breakdown voltage, the bottom layer of the bypass diode having said first polarity.

48. (Previously submitted) A device as defined in claim 47, wherein the sequence of layers of one of said cells and the sequence of layers of the bypass diode are epitaxially grown in the same process step.

49. (Previously submitted) A device as defined in claim 47, wherein the semiconductor body includes a Ge substrate, and at least one of the solar cells is fabricated at least in part with GaAs.

50. (Currently amended) A solar cell semiconductor device comprising:

a semiconductor structure having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiconductor material forms a

sequence of subcells of a multijunction solar cell where the top layer of the top subcell has a first polarity; and

a second region separated from said first region by a trough in said sequence of layers and in which the sequence of layers forms a support for an integral bypass diode to protect the multijunction solar cell against reverse biasing by allowing current to pass when the solar cell is shadowed where the bottom layer of the bypass diode has the same polarity as said first polarity of said top subcell; wherein

the bypass device and the subcell have an identical ~~sequences~~ sequence of semiconductor layers where each layer in the bypass device has substantially the same composition and thickness as the corresponding layer in the subcell ~~with substantially the same thickness~~ ~~with substantially the same thickness~~ and form an integral semiconductor body.

51. (Previously submitted) A device as defined in claim 50, wherein the sequence of layers of semiconductor material and the sequence of layers of the bypass diode are epitaxially grown in a different process step.

52. (Previously submitted) A device a defined in claim 50, wherein the semiconductor structure includes a Ge substrate, and at least one of the cells is fabricated at least in part with GaAs.

53. (Previously submitted) A device as defined in claim 50, further comprising

a lateral conduction layer lying over said layers of said second region for electrically connecting the multijunction solar cell to said bypass diode.

54. (Previously submitted) The device as defined in claim 53, wherein said structure includes a substrate, wherein the subcells are formed on a first portion of the substrate and said bypass diode is formed on a second portion of the substrate over said lateral conduction layer.

55. (Previously submitted) The device as defined in claim 53, wherein the solar cell and lateral conduction layer are epitaxially grown in a first process and the active layers of said bypass diode are epitaxially grown in a subsequent second process.

56. (Previously submitted) The device as defined in claim 55, wherein said epitaxially grown diode is electrically connected across at least first and second of said subcells to protect such first and second subcells against reverse biasing at less than breakdown voltage.

57. (Previously submitted) The device as defined in claim 50, wherein the bypass diode includes a metal/semiconductor contact.

58. (Previously submitted) The device as defined in claim 57, wherein the metal/semiconductor contact is TiAu with InGaP.

59. (Previously submitted) The device as defined in claim 57, wherein the metal/semiconductor contact forms a Schottky junction.

60. (Previously submitted) The device as defined in claim 50, wherein said bypass diode includes p-type, i-type, and n-type layers.

61. (Previously submitted) The device as defined in claim 53, wherein the lateral conduction layer is an n-doped GaAs layer for conducting electrical current.

62. (Previously submitted) The solar device of claim 60, wherein the p-type layer of the bypass diode is a p-doped GaAs layer and the n-type layer of the bypass diode is an n-doped GaAs layer.

63. (Previously submitted) The solar device of claim 60, wherein the i-type layer of the bypass diode is a lightly doped GaAs layer for reducing defect breakdown.

64. (Previously submitted) The solar device of claim 60, wherein the i-type layer of the bypass diode is an undoped GaAs layer for reducing defect breakdown.

65. (Currently amended) A solar cell semiconductor device comprising:

a substrate;

a first sequence of layers of semiconductor material deposited on said substrate, including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell where the top layer of the top cell has a first polarity; and

a second region including said first sequence of layers, and a second sequence of layers that forms a bypass diode to protect said at least one cell against reverse biasing at less than breakdown voltage where the bottom layer of the bypass diode has the same polarity as said first polarity of said top cell; and

a metal layer deposited on a portion of said substrate and over at least a portion of said second region for electrically shorting the first sequence of layers of said second region and to electrically connect to said bypass diode in said second region.

66. (Previously submitted) A device as defined in claim 65, further comprising a lateral conduction layer wherein said metal layer forms a shunt having a first contact on the solar cell and a second contact on the bypass diode, wherein said first contact is connected to the substrate to make an electrical connection to the solar cell and said second contact is connected to a lateral conduction layer to make an electrical connection to the bypass diode.

67. (Previously submitted) A device as defined in claim 65, further comprising a trough situated between the solar cell and the bypass diode that provides electrical isolation between the solar cell and the diode.

68. (Previously submitted) A device as defined in claim 66, further comprising a stop etch layer deposited over the lateral conduction layer.

69. (Previously submitted) A device as defined in claim 65, wherein said bypass diode includes p-type, i-type, and n-type layers.

70. (Previously submitted) A device as defined in claim 66, wherein the lateral conduction layer is an n-doped GaAs layer for conducting electrical current.

71. (Previously submitted) A device as defined in claim 69, wherein the p-type layer of the bypass diode is a p-doped GaAs layer and the n-type layer of the bypass diode is an n-doped GaAs layer.

72. (Previously submitted) A device as defined in claim 69, wherein the i-type layer is a lightly doped GaAs layer for reducing defect breakdown.

73. (Previously submitted) A solar device as defined in claim 69, wherein the i-type layer is an undoped GaAs layer for reducing defect breakdown.

74-85. (Cancelled)

86. (Currently amended) An integrated semiconductor structure comprising:

a multijunction solar cell including first and second solar cells on a first portion of the semiconductor structure;

means integral to a second portion of said semiconductor structure overlying said second portion for passing current when said multijunction solar cell is shaded; and

a metal layer connecting said multijunction solar cell and said means for passing current, wherein one end of said metal layer is coupled to a base of said first solar cell and another end of said metal layer is coupled to one terminal of said means for passing current; wherein

the top layer of the top cell has a first polarity; and

the bottom layer of the bypass diode has the same polarity as said first polarity of said top layer of the top cell.

87. (Previously submitted) The structure as structure as defined in claim 86, wherein said first solar cell is formed on a first portion of the substrate, and said means for passing current is a bypass diode formed on a second portion of the substrate.

88. (Previously submitted) The structure as defined in claim 87, wherein said first portion and said second portion are separated by a trough, and said metal layer lies over said trough.

89. (Previously submitted) The structure as defined in claim 86, wherein said first and second solar cells are grown in a first process and said bypass diode is formed in a subsequent process.

90. (Currently amended) A solar cell semiconductor device comprising:

an integral semiconductor body having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiconductor material forms a sequence of cells of a multijunction solar cell, with the top layer of the top cell having a first polarity; and

a second region laterally spaced apart from said first region and in which the sequence of layers corresponding to the sequence of layers forming said cells forms a support structure for a bypass diode to protect said multijunction solar cell against reverse biasing at less than breakdown voltage, said bypass diode comprising at least one layer, wherein the bottom layer of the bypass diode has the same polarity as said first polarity of said top layer of said top cell.

91. (Previously submitted) A device as defined in claim 90, wherein the sequence of layers of said multijunction solar cell and the sequence of layers of the support structure are formed in the same process step.

92. (Previously submitted) A device as defined in claim 90, wherein the bypass diode is fabricated at least in part with GaAs.

93. (Currently amended) A solar cell semiconductor device comprising:

a substrate;

a sequence of layers of material deposited on said substrate, including a first region in which the sequence of layers of material forms a plurality of cells of a multijunction solar cell, and a second region in which the sequence of layers corresponding to the sequence of layers forming said cells forms a support for a bypass diode to protect said cell against reverse biasing; and

a planar lateral conduction layer deposited over the sequence of layers in the second region for making electrical contact to an active region of said bypass diode; wherein

the topmost layer of the topmost cell has a first polarity; and

the bottom layer of the bypass diode has the same said first polarity as said topmost layer of said topmost cell.

94. (Currently amended) A device as defined in claim 93, further comprising:

a lateral conduction layer deposited over the sequence of layers in the first region;

wherein said lateral conduction layer in the first region is physically separated from the lateral conduction layer in the second region.

95. (Previously submitted) A device as defined in claim 93, wherein said lateral conduction layer is a highly doped layer.

96. (Previously submitted) A device as defined in claim 95, wherein said lateral conduction layer is composed of GaAs.

97. (Previously submitted) A device as defined in claim 93, further comprising an etch stop layer, deposited over said lateral conduction layer.

98. (Previously submitted) A device as defined in claim 93, wherein said substrate forms an electrical connection path between said multijunction solar cell as said bypass diode.

99. (Previously submitted) A device as defined in claim 93, further comprising

a metal layer deposited on a portion of said substrate and over at least a portion of said second region and functioning to (i) electrically short layers of said second region, and (ii) connect the substrate to said lateral conduction layer to complete the electrical circuit between the multijunction solar cell and the bypass diode.

100. (Currently amended) A solar cell semiconductor device comprising:

a substrate;

a sequence of layers of semiconductor material deposited on said substrate including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell, and a second region in which a sequence of layers corresponding to the sequence of layers forming said at least one cell, forms a bypass diode to protect said cell against reverse biasing; and

wherein the sequence of layers in the first and second regions includes a lateral conduction layer including a first portion disposed in said first region, and a second portion disposed in said second region and physically separated from said first portion and further wherein:

the topmost layer of the topmost cell has a first polarity; and

the bottom layer of the bypass diode has the same polarity as said first polarity of said topmost cell.

101. (Previously submitted) A device as defined in claim 100, wherein said lateral conduction layer is a highly doped layer.

102. (Previously submitted) A device as defined in claim 100, wherein said lateral conduction layer is composed of GaAs.

103. (Previously submitted) A device as defined in claim 100, wherein one of the layers of said sequence of layers is a cap layer, and said lateral conduction layer is disposed directly over said cap layer.

104. (Previously submitted) A device as defined in claim 100, wherein said second portion of said lateral conduction layer makes electrical contact with a layer of said bypass diode.

105. (Previously submitted) A device as defined in claim 100, wherein said bypass diode comprises an n GaAs layer, and a p GaAs layer disposed over said n GaAs layer.

106. (Previously submitted) A device as defined in claim 100, further comprising a metal layer deposited on a portion of said substrate and over at least a portion of said second region and functioning to connect the substrate to a portion of said lateral conduction layer for completing the electrical circuit between the multijunction solar cell and the bypass diode.

107. (Currently amended) A solar cell semiconductor device comprising:

a substrate;

a sequence of layers of semiconductor material deposited on said substrate, including a first region in which a lower portion of said sequence of layers of semiconductor material forms a multijunction solar cell, and a second region in which an upper portion of said sequence of layers forms a bypass diode to protect said cell against reverse biasing at less than breakdown voltage; and

a highly conductive lateral conduction layer deposited over the portion of said sequence of layers forming the multijunction solar cell, for making electrical contact with one layer of said bypass diode and forming a contact region to allow said bypass diode to be electrically connected to said multijunction solar cell; wherein

the topmost layer of the topmost cell has a first polarity; and

the bottom layer of the bypass diode has the same polarity as said first polarity of said topmost cell.

108. (Previously submitted) A device as defined in claim 107, further comprising a metal layer deposited on a portion of said substrate and over at least a portion of said second region and functioning to connect the substrate to a portion of said lateral conduction layer for completing the electrical circuit between the multijunction solar cell and the bypass diode.

109. (Previously submitted) A device as defined in claim 107, wherein said lateral conduction layer includes a first portion disposed in said first region, and a second portion disposed in said second region and separated from the first portion.

110. (Previously submitted) A device as defined in claim 107, wherein said lateral conduction layer is composed of GaAs.

111. (Previously submitted) A device as defined in claim 109, wherein said second portion of said lateral conduction layer makes electrical contact with a first active layer of said bypass diode.